



UNITED STATES PATENT AND TRADEMARK OFFICE

Sr

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/050,233	01/16/2002	Robert E. Stengel	CM03359J	6380

7590 04/21/2005

Andrew S. Fuller
Motorola, Inc.
Law Department
8000 West Sunrise Boulevard
Fort Lauderdale, FL 33322

EXAMINER

WONG, LINDA

ART UNIT PAPER NUMBER

2634

DATE MAILED: 04/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/050,233

Applicant(s)

STENGEL ET AL.

Examiner

Linda Wong

Art Unit

2634

– The MAILING DATE of this communication appears on the cover sheet with the correspondence address –
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 16 January 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-80 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 52-60, 79 and 80 is/are allowed.
- 6) ☒ Claim(s) 1, 2, 6-8, 11-34, 36-40, 45-50, 61-71 and 73 is/are rejected.
- 7) ☒ Claim(s) 3-5, 9, 10, 35, 41-44, 51, 72 and 74-78 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 16 January 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. **Claim 7** recites the limitation "the second tap selection circuit" in claim 6. There is insufficient antecedent basis for this limitation in the claim.
2. **Claim 8** recites the limitation "the first tap selection processor" in claim 8. There is insufficient antecedent basis for this limitation in the claim.
3. **Claim 9** recites the limitation "the second tap selection processor" in claim 9. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. **Claims 11 - 19** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claims are inconsistent with the specifications.
 - a. **Claim 11**, based on the specification, Φ is the phase shift expressed as a fraction of wavelength = $\alpha/(\pi/2)$ and $\Phi = \alpha/(\pi/2) * K.C.$. Claim 11 recites $\Phi = K.C.$, and Φ is the desired phase shift, which is inconsistent with the specification.

- b. **Claim 15**, based on the specification, α is $\pi/2$ radians phase offset of the normalized ratio of F_{ref}/F_{out} . Thus, the amount of delay added to the tap address would be $\alpha/(\pi/2)$. Also, it should be clarified that α is the desired phase shift in radians.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. **Claims 1, 2, 6, 7, 8, 49, 50** are rejected under 35 U.S.C. 103(a) as being unpatentable over Bockelman₁ (US Publication No.: 20020110211) in view of Nakase et al. (US Publication No.: 20020059352)
- a. **Claim 1**, Bockelman₁ discloses a delay locked loop comprising a plurality of tap outputs (Fig. 2, labels 38, 46, 48, 36, and 16), a first and second selection circuit comprised of producing first and second set of tap addresses (Fig. 8, output from label 20, output from label 60 and pg. 2, paragraph [0019], lines 8-9) to select a first and second set of plurality of tap outputs from a delay line (Fig. 8, labels 16, 18, 56 and 58) to produce a first and second output signal (Fig. 8, output from label 18 and 58). Although Bockelman₁ does not disclose two timings used for the selection of a plurality of tap outputs from a delay line,

Nakase et al. discloses a delay line with two selections based on timings. (Fig. 1, labels clk 2, 20 and 21) It would be obvious to one skilled in the art to apply the use of timings disclosed by Nakase et al to Bockelman₁'s process of outputting phase shifts of a clock signal to produce different tap addresses at different timings, providing outputs with different shifts.

- b. **Claim 2**, Although Bockelman₁ does not disclose a modulator, Nakase et al disclose a modulator combining the first and second output signals to produce a modulated signal. (Fig. 1, output from labels 30, 31, 32, 40 and output L3) As explained in the specification of the applicant and recited in this claim, in Fig. 10 the modulated signal is produced by combining the outputs from the first and second selection circuit. Thus, although Nakase et al does not explicitly disclose that the output L3 as a modulated signal, based on the description provided by the applicant, Nakase et al's output is equal to the modulated signal disclosed by the applicant.
- c. **Claims 6 and 7**, Bockelman₁ discloses a first and second tap selection processor that selects the first set of the plurality of tap outputs from the delay line and a first and second demultiplexor responsive to the first and second tap selection processor to selectively route the selected first set of tap outputs to a common node to produce the first output signal (Fig. 8, labels 16, 18, 20, 56, 58, 60 and pg. 2, paragraph [0019], lines 8-15) Although Bockelman₁ does not disclose a first and second timing, Nakase et al discloses selections based on timings. (Fig. 1, labels clk 2, 20 and 21) It would be obvious to one skilled in

the art to apply the use of timings disclosed by Nakase et al to Bockelman₁'s process of outputting phase shifts of a clock signal to produce different tap addresses at different timings, providing outputs with different shifts.

- d. **Claim 8** inherits all the limitations of claims 6 and 7.
 - e. **Claim 49, 50** inherits all the limitations of claim 1. F_{out1} and F_{out2} are equivalent to the outputs from label 18 and 58 in Fig. 8.
6. **Claims 20-34, 36-40, 45-48, 61-71, 73** are rejected under 35 U.S.C. 103(a) as being unpatentable over Bockelman₁ (US Publication No.: 20020110211) in view of Bockelman₂ et al. (US Patent No.: 6353649)
- a. **Claim 20**, Bockelman₁ discloses a delay locked loop with a plurality of delay or tap outputs. Although Bockelman₁ does not disclose a tap selection processor as recited in the claim, Bockelman₂ et al. discloses a tap selection processor providing tap addresses or numbers (Col. 4, line 20-21) as outputs according to a modulating signal. (Fig. 5, labels 506, 302, 306, 304, 508, 502, 504) It would be obvious to one skilled in the art to apply Bockelman₂ et al. to Bockelman₁'s invention to reduce complexity and power consumption. (Col. 4, lines 39-40)
 - b. **Claim 21**, Bockelman₂ et al discloses a multiplexor circuit and tap addresses applied to the multiplexor to select a time varying sequence of tap outputs as an output signal $F_{out}(t)$. (Fig. 5, output from label 502 and label DLL and D:1)
 - c. **Claims 22, 23, 24, 25**, Bockelman₂ et al does not explicitly disclose the tap addresses are selected to amplitude, phase or frequency modulate the output

- signal by the modulating signal, the modulation input is inherently any modulated signal or any combination of types of modulation signal.
- d. **Claims 26, 27** Bockelman₂ et al does not distinctly claim an analog or data modulated signal, Bockelman₂ et al inherently discloses a modulating signal with an analog signal and data signal since modulated signal are computed by adding a carrier signal to some incoming, digital or analog signal composed of data.
 - e. **Claim 28** inherits all the limitations of claims 20, 21 and 23.
 - f. **Claim 29**, Bockelman₂ et al disclose an adder adding the modulating signal to taps address. (Fig. 5, label 502, 504)
 - g. **Claims 30, 31**, Bockelman₂ et al disclose an output based on the tap addressed outputted from adder 502, wherein the adder adds a modulation signal to the tap addresses. It is inherent that the output signal would be selected to amplitude or phase or frequency modulated the output signal since the selection is based on modulated signals. As explained in the rejection of claims 22-25, Bockelman₂ et al does not specify an modulation scheme, thus Bockelman₂ inherently discloses a phase or frequency or amplitude modulation signal.
 - h. **Claims 32 and 33** inherit all the limitations of claims 26 and 27.
 - i. **Claim 34** inherits all the limitations of claims 20, 21 and 24.
 - j. **Claim 36** inherits all the limitations of claim 22.
 - k. **Claim 37** inherits all the limitations of claim 23.

- l. **Claims 38 and 39** inherit all the limitations of claims 26 and 27.
- m. **Claim 40** inherits all the limitations of claim 20 and 30.
- n. **Claim 45** inherits all the limitations of claim 24.
- o. **Claim 46** inherits all the limitations of claim 23.
- p. **Claim 47 and 48** inherit all the limitations of claim 26 and 27.
- q. **Claim 61**, Bockelman₁ disclose a delay locked loop having a delay line with a plurality of tap outputs (Fig. 2, labels 38, 46, 48, 36). Although Bockelman₁ does not disclose receiving a modulating signal and selecting a sequence of tap addresses varying in accordance with the modulating signal, Bockelman₂ et al disclose a modulating signal (Fig. 5, label 504) and tap addresses varying according to the modulating signal. (Fig. 5, labels 504, output from label 502)
- r. **Claim 62** inherits all the limitations of claim 21.
- s. **Claim 63** inherits all the limitations of claim 22.
- t. **Claim 64** inherits all the limitations of claim 23.
- u. **Claim 65** inherits all the limitations of claim 24.
- v. **Claim 66** inherits all the limitations of claim 25.
- w. **Claims 67 and 68** inherit all the limitations of claims 26 and 27.
- x. **Claim 69** inherits all the limitations of claims 61 and 23.
- y. **Claim 70** inherits all the limitations of claim 29.
- z. **Claim 71** inherits all the limitations of claim 61 and 24.
- aa. **Claim 73** inherits all the limitations of claim 61.

Art Unit: 2634

Allowable Subject Matter

7. **Claims 3-5, 9-10, 35, 41, 42, 43, 44, 51, 72, 74-78** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claim 9 must be rewritten to overcome all objections.
8. **Claims 11-19** would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.
9. **Claims 52-60, 79-80** are allowed.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linda Wong whose telephone number is 571-272-6044. The examiner can normally be reached on 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on (571) 272-3056. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LW


STEPHEN CHIN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800